

Appl. No. 09/741,616  
Amdt. dated Feb. 10, 2005  
Reply to Office action of Jan. 18, 2006

### **REMARKS/ARGUMENTS**

Claims 1-38 remain in the application. The examiner rejected claims 1-10, 12-29 and 31-38, and objected to claims 11 and 30 in the Office Action mailed January 18, 2006 (hereinafter referred to as "Office Action"). The claim amendments are supported in the drawings and original specification. Accordingly, applicants respectfully submit that no new matter is added. In view of the following remarks and amendments, applicants respectfully request a timely Notice of Allowance be issued in this case.

#### ***Rejections under 35 U.S.C. § 103(a)***

The examiner rejected: (1) claims 1-2, 8-10, 13-19, 20-21, 23-27, 31, 35-8 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,651,123 to Nakagawa et al. in view of U.S. Patent No. 5,781,470 to Sourgen et al.; (2) claims 3-4 under 35 U.S.C. § 103(a) as being unpatentable over Nakagawa in view of Sourgen and further in view of U.S. Patent No. 5,490,280 to Gupta et al.; and (3) claims 5-7, 22, 28-29 and 32-34 under 35 U.S.C. § 103(a) as being unpatentable over Nakagawa in view of Sourgen and further in view of U.S. Patent No. 5,530,837 to Williams et al.

In order to establish a prima facie case of obviousness, three criteria must be met: (1) there must be some suggestion or motivation in the prior art to modify the reference or to combine reference teachings as proposed, (2) there must be a reasonable expectation of success, and (3) the prior art or combined references must teach or suggest all the claim limitations. MPEP § 2143; *In re Vacek*, 947 F.2d 488 (Fed. Cir. 1991). "The prior art must suggest the desirability of the claimed invention." MPEP § 2143.01. **Both the invention and the prior art references must be considered as a whole.** MPEP § 2141.02. Applicants respectfully submit that claims 1-38, as amended, are not obvious over the cited art and are, therefore, allowable under 35 U.S.C. § 103(a) for the reasons stated below.

#### ***There is no suggestion or motivation to modify or combine the references***

As shown in Figure 4 and throughout Nakagawa (e.g., col. 7, lines 25-32), Nakagawa uses a pseudo-random number program counter (30) to output instruction addresses that are to be read next from instruction memory (32) by instruction decoder (34). As a result, the pseudo-random number program counter (30) works with instructions prior to decoding by the instruction decoder (34). In addition, the pseudo-random number program counter (30) outputs one address for one instruction.

As shown in Figure 2, Sourgen discloses a pseudo random generator (8) connected to a microprocessor ( $\mu$ p) and a counter (9) that delays, for a random time period, the execution of a write instruction to a memory cell (col. 5, lines 58-62; col. 6, lines 5-6). The purpose of Sourgen is to protect the memory cell (col. 4, lines 27-39); not

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allocate resources. Moreover, the pseudo random generator (8) is not within the microprocessor ( $\mu$ p). Applicants respectfully submit that there is no suggestion or motivation to take a memory write delay circuit that is exterior to a microprocessor and place the circuit within the microprocessor and then use a delay circuit to somehow allocate resources. As a result, Sourgen does not cure the deficiencies of Nakagawa.

As shown in Figure 1B, Gupta discloses a reorder buffer (507) downstream from the instruction decode (521). Applicants respectfully submit that there is no suggestion or motivation to take a post instruction decode reorder buffer and incorporate it into Nakagawa's pre-instruction decode pseudo-random number program counter (30). Moreover, even if such a combination were made, it would not disclose, teach or suggest the inventions recited in claims 1-38, as amended, because such a combination would be upstream of the instruction decode. As a result, Gupta does not cure the deficiencies of Nakagawa.

As shown in the Abstract, Williams discloses a method of allocating memory in an arbitrary number of memory banks. Williams does not disclose allocating memory within a microprocessor. Applicants respectfully submit that even if the memory allocation method of Williams was combined with Nakagawa's pre-instruction decode pseudo-random number program counter (30), it would not disclose, teach or suggest the inventions recited in claims 1-38, as amended, because such a combination would be upstream of the instruction decode. As a result, Williams does not cure the deficiencies of Nakagawa.

Accordingly, applicants respectfully submit that claims 1-38, as amended, are not obvious over the cited art and are, therefore, allowable under 35 U.S.C. § 103(a). Accordingly, applicants respectfully request that the rejection of claims 1-38 be withdrawn.

***There is no reasonable expectation of success***

For the reasons stated above, applicants respectfully submit that there is no reasonable expectation of success to modify Nakagawa using the teachings of Sourgen, Gupta or Williams. As a result, applicants respectfully submit that claims 1-38, as amended, are not obvious over the cited art and are, therefore, allowable under 35 U.S.C. § 103(a). Accordingly, applicants respectfully request that the rejection of claims 1-38 be withdrawn.

***The cited references do not teach or suggest all the claim limitations***

Unless the reference(s) teach or suggest all the claim limitations, obviousness cannot be found. MPEP § 2143.03. Further, once an independent claim is found to be non-obvious under 35 U.S.C. § 103, then any claim which depends from that independent claim is also non-obvious. MPEP § 2143.03; *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

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For the reasons stated below, applicants respectfully submit that the cited references do not disclose, teach or suggest all the claim elements of claims 1-38, as amended.

***Claims 1, 20, 31 and 38***

With respect to claims 1, 20, 31 and 38, as amended, applicants respectfully submit that Nakagawa, Sourgen and the other references, either alone or in combination, do not disclose, teach or suggest all the claimed elements. More specifically, the cited references do not disclose, teach or suggest:

- (1) an apparatus or method that allocates one or more resources within a microprocessor to a decoded instruction wherein each resource identifier corresponds to one of the resources within the microprocessor; or
- (2) a resource identifier selector within the microprocessor or method that determines how many of the resource identifiers, if any, are required by the decoded instruction and selects one or more of the resource identifiers within for allocation to the decoded instruction.

As recognized by the examiner, and as shown in Figure 4 and throughout Nakagawa (e.g., col. 7, lines 25-32), Nakagawa uses a pseudo-random number program counter (30) to output instruction addresses that are to be read next from instruction memory (32) by instruction decoder (34). As a result, Nakagawa does not disclose, teach or suggest an apparatus that allocates one or more resources within a microprocessor to a decoded instruction. Likewise, Nakagawa does not disclose, teach or suggest selecting one or more of the resource identifiers for allocation to the decoded instruction.

In addition, the pseudo-random number program counter (30) outputs one address for one instruction. As a result, Nakagawa does not disclose, teach or suggest does not determine how many of the resource identifiers, if any, are required by the decoded instruction and selects one or more of the resource identifiers for allocation to the decoded instruction. As claimed, the present invention can select zero, one or more resource identifiers for allocation to the decoded instruction.

Sourgen does not cure the deficiencies of Nakagawa because: (1) Sourgen does not allocate resources when it protects the memory cell by delaying execution of the write signal (col. 4, lines 27-39); and (2) the pseudo random generator (8) is not within the microprocessor ( $\mu$ p). Applicants respectfully submit that there is no suggestion or motivation to take a memory write delay circuit that is exterior to a microprocessor and place the circuit within the microprocessor and then use a delay circuit to some how allocate resources.

Accordingly, applicants respectfully submit that Nakagawa, Sourgen, Gupta, Williams and the other cited references, either alone or in combination, do not disclose, teach or suggest all the claimed elements in claims 1, 20, 31 and 38, as amended. As a

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result, applicants respectfully submit that claims 1, 20, 31 and 38, as amended, are not obvious over the cited references and are, therefore, allowable under 35 U.S.C. § 103(a). Applicants respectfully request that the rejection of claims 1, 20, 31 and 38, as amended, be withdrawn.

***Claims 2-10, 12-19, 21-29 and 31-37***

Applicants respectfully submit that claims 2-10, 12-19, 21-29 and 31-37 depend from claims 1, 20 and 31, respectively, which are allowable for the reasons stated above, and further distinguish over the cited references. Claims 2-10, 12-19, 21-29 and 31-37 are, therefore, allowable under 35 U.S.C. § 103(a). Accordingly, applicants respectfully request that the rejection of claims 2-10, 12-19, 21-29 and 31-37 be withdrawn.

***Claims 11 and 30***

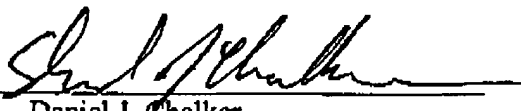
Applicants acknowledge the objection to claims 11 and 30 as being dependent upon a rejected base claim and that they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

For the reasons set forth above, applicants respectfully request reconsideration by the Examiner and withdrawal of the rejections. Applicants submit that claims 1-38, as amended, are fully patentable. Applicants respectfully request that a timely Notice of Allowance be issued in this case. If the Examiner has any questions or comments, or if further clarification is required, it is requested that the Examiner contact the undersigned at the telephone number listed below.

Respectfully submitted,

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